

IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in this application:

Claim 1 (Currently Amended): A method for synchronizing two or more graphics processing units, comprising:

- receiving a clock signal from a clock generator of a first graphics processing unit (GPU) and an external synchronization signal;

- determining whether the phase of the clock signal and the phase of the external synchronization signal are synchronized;

- adjusting the frequency of the clock generator to the frequency of the external synchronization signal if the phases of the clock signal and the external synchronization signal are not synchronized to generate a synchronized timing signal;

- transmitting the synchronized timing signal to a second graphics processing unit (GPU); and

- producing an image for synchronous output to multiple displays using the synchronized timing signal, including the steps of:

 - generating a first portion of an image in the first graphics unit and generating a second portion of the image in the second graphics processing unit such that the first portion and the second portion synchronously form the image, and

 - transmitting the synchronized timing signal to the first graphics processing unit and the second graphics processing ~~module~~ unit in response to the clock signal and the synchronization signal being in phase to control the generation of the first and second images image portions.

Claim 2 (Previously Presented): The method of claim 1, further comprising transmitting the synchronized timing signal from the second graphics processing unit to a third graphics processing unit.

Claim 3 (Previously Presented): The method of claim 1, further comprising:

- determining whether a first stereo field signal of the first graphics processing unit and a second stereo field signal of the second graphics processing unit are

synchronized; and

adjusting the phase of the second stereo field signal to the phase of the first stereo field signal if the first stereo field signal and the second stereo field signal are not synchronized to generate a synchronized stereo field signal.

Claim 4 (Previously Presented): The method of claim 3, further comprising transmitting the synchronized stereo field signal from the second graphics processing unit to a third graphics processing unit.

Claim 5 (Previously Presented): The method of claim 1, further comprising synchronizing a swap ready signal of the second graphics processing unit with a swap ready signal of the first graphics processing unit.

Claim 6 (Previously Presented): The method of claim 5, wherein synchronizing the swap ready signal of the second graphics processing unit with the swap ready signal of the first graphics processing unit comprises:

receiving a frame divider;

triggering a new video start address in a memory; and

determining whether a swap ready element on at least one of the graphics processing units is logically true.

Claim 7 (Original): The method of claim 6, further comprising scanning out data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true.

Claim 8 (Original): The method of claim 6, further comprising, prior to determining whether the swap ready element on the at least one of the graphics processing units is logically true:

determining whether the current scanline is within a video blanking interval; and

scanning out the data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true and the current scanline is within the video blanking interval.

Claim 9 (Original): The method of claim 6, further comprising performing a series of

video memory block transfers if the swap ready element on the at least one of the graphics processing units is logically true.

Claim 10 (Original): The method of claim 6, further comprising, prior to determining whether the swap ready element on the at least one of the graphics processing units is logically true:

- determining whether the current scanline is within a video blanking interval; and
- performing the series of video memory block transfers if the swap ready element on the at least one of the graphics processing units is logically true and the current scanline is within the video blanking interval.

Claim 11 (Original): The method of claim 6, wherein the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of the graphics processing units is ready to be transferred to a front portion of the frame buffer.

Claim 12 (Original): The method of claim 6, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical HIGH state.

Claim 13 (Original): The method of claim 6, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical LOW state.

Claim 14 (Original): The method of claim 1, wherein the first graphics processing unit and the second processing unit are implemented on one of a silicon substrate, a printed circuit board, and an array of display elements.

Claims 15 - 30 (Canceled)

Claim 31 (Currently Amended): An apparatus for synchronizing two or more graphics processing units, comprising:

- means for receiving a clock signal from a clock generator of a first graphics processing unit and an external synchronization signal;

- means for determining whether the phase of the clock signal and the phase of the external synchronization signal are synchronized;

means for adjusting the frequency of the clock generator to the frequency of the external synchronization signal if the phases of the clock signal and the external synchronization signal are not synchronized to generate a synchronized timing signal;

means for transmitting the synchronized timing signal to a second graphics processing unit; and

means for producing an image for synchronous output to multiple displays using the synchronized timing signal,

wherein the first graphics processing unit is configured to generate a first portion of an image, and the second graphics processing unit is configured to generate a second portion of the image such that the first portion and the second portion synchronously form the image, and

wherein the controller is configured to transmit the synchronized timing signal to the first graphics processing unit and the second graphics processing ~~module~~ unit in response to the clock signal and the synchronization signal being in phase to control the generation of the first and second ~~images~~ image portions.

Claim 32 (Previously Presented): The apparatus of claim 31, further comprising:

means for determining whether a first stereo field signal of the first graphics processing unit and a second stereo field signal of the second graphics processing unit are synchronized; and

means for adjusting the phase of the second stereo field signal to the phase of the first stereo field signal if the first stereo field signal and the second stereo field signal are not synchronized.

Claim 33 (Previously Presented): The apparatus of claim 31, further comprising means for synchronizing a swap ready signal of the second graphics processing unit with a swap ready signal of the first graphics processing unit.

Claim 34 (Previously Presented): The method of claim 1, further comprising:

receiving a second clock signal from a clock generator of the second graphics processing unit;

determining whether the phase of the second clock signal of the second graphics

processing unit and the phase of the synchronized timing signal received from the first graphics processing unit are synchronized;

adjusting the frequency of the clock generator to the frequency of the external synchronization signal if the clock signal and the external synchronization signal are not synchronized to generate a synchronized second clock signal; and

producing a portion of the image using the synchronized second clock signal.

Claim 35 (Previously Presented): The apparatus of claim 31, further comprising means for indicating visually that the synchronization timing signal is transmitted from the first graphics processing unit to the second graphics processing unit.

Claim 36 (Previously Presented): A method as claimed in claim 1 including:

setting a swap ready element at each of the first and second GPUs to control an immediate series of video memory block transfers at each of the first and second GPUs whose timing is controlled by the synchronized timing signal at each of first and second GPUs.

Claim 37 (Previously Presented): The apparatus as claimed in claim 31 wherein the means for producing and image is configured to:

set a swap ready element at each of the first and second GPUs to control an immediate series of video memory block transfers at each of the first and second GPUs whose timing is controlled by the synchronized timing signal at each of first and second GPUs.